IN THE CLAIMS:

Kindly amend claims 12, 20 and 22 as follows.

Kindly replace claim 12 with the following amended claim 12:

12. (Amended) A method of manufacturing a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating surfaces;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a conductive layer on the interlevel insulating layer and in the first and second via holes;

etching back the conductive layer to form: (i) a conductive sidewall spacer on the conductive layer formed in the first via hole and on the sidewalls of the first via hole for preventing dielectric disconnection; (ii) a conductive plug in the second via hole; and (iii) an exposed surface containing the spacer, conductive plug, the predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the conductive sidewall spacer and the conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the conductive sidewall spacer and predetermined surface of the lower electrode; and

cont.

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simultaneously forming: (i) a second wire line connected to the conductive plug; and (ii) an upper electrode connected to the dielectric layer.

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

12. (Amended) A method of manufacturing a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating surfaces;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a conductive layer on the interlevel insulating layer and in the first and second via holes;

etching back the conductive layer to form: (i) a conductive sidewall spacer on the conductive layer formed in the first via hole and on the sidewalls of the first via hole for preventing dielectric disconnection; (ii) a conductive plug in the second via hole; and (iii) an exposed surface containing the spacer, conductive plug, the predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the conductive sidewall spacer and the conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the conductive sidewall spacer and predetermined surface of the lower electrode; and

simultaneously forming: (i) a second wire line connected to the conductive plug; and (ii) an upper electrode connected to the dielectric layer.

Replace claim 20 with the following amended claim:

20. (Twice Amended) The method as claimed in claim 19, wherein the anti-reflection layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, Mo, TiN, TiW, TaN, and MoN and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N.

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

20. (Twice Amended) The method as claimed in claim 19, wherein the anti-reflection layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, Mo, TiN, TiW, TaN, and MoN[;] and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N[; and (iii) combination layers thereof].

Replace claim 22 with the following amended claim:

22. (Amended) The method as claimed in claim 21, wherein the metal barrier layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, Mo, TiN, TiW, TaN, and MoN and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N.

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

22. (Amended) The method as claimed in claim 21, wherein the metal barrier layer has a structure selected from the group consisting of: (i) a single-level structure comprised of one or more materials selected from the group consisting of Ti, Ta, Mo, TiN, TiW, TaN, and MoN[;] and/or (ii) a multi-level structure comprised of one or more materials selected from the group consisting of W-N, W-Si-N, Ta-Si-N, W-B-N, and Ti-Si-N[; and (iii) combination layers thereof].